



A Charutar Vidya Mandal's Institution
V.P. & R.P.T.P. SCIENCE COLLEGE
(AUTONOMOUS) (Grant-in-Aid)
Affiliated to Sardar Patel University
VALLABH VIDYANAGAR-388120



Bachelor of Science Semester 5 Internal Examination - 2025

COURSE CODE : US05MAPHY02 COURSE TITLE: Analog & Digital Circuit

Date: 23-09-2025 Tuesday

Time: 10:45 to 12:15 pm

Marks: 30

Q. 1 Answer with correct option: (Each of 1 Mark)

(6)

1. The optimum conversion efficiency in Class B push-pull circuit is %.
(a) 60 (b) 78.5 (c) 25 (d) 50
2. A Class B push-pull complementary symmetry amplifier requires ...
(a) one transformer (b) two transformers
(c) three transformer (d) no transformer
3. The bandwidth of an ideal op-amp is
(a) infinite (b) zero (c) very low (d) constant
4. The binary 1101 is equivalent to decimal number...
(a) 12 (b) 13 (c) 26 (d) 25
5. How many NAND gates are used to form an AND gate?
(a) 1 (b) 2 (c) 3 (d) 4
6. When both inputs of SR NAND latch are high, then output will be....
(a) No change (b) Race (c) Set (d) Reset

Answer in detail. (Each of 6 Mark)

(24)

- Q.2** Draw labeled circuit of an Approximate high-frequency circuit for determination of short-circuit CE current gain and discuss β cut-off frequency (f_β) and α cut-off frequency (f_α).

OR

Draw labeled diagram of a Class A push-pull amplifier. Using theory of its operation explain how harmonics distortion is reduce at its output.

- Q.3** Draw circuit symbol of an ideal op-amp. State characteristics of ideal op-amp and obtain expressions for close loop voltage gain of ideal inverting op-amp.

OR

Explain op-amp. as (i) Summng amplifier (ii) Integrator circuit.

- Q.4** Explain how to build three input OR and AND gates using diodes and explain their truth table.

OR

Discuss the two input NOR and NAND gates with logic symbol and truth table. Also discuss the De-Morgan's theorems.

- Q.5.** Explain the working of 4-bit Shift-Left register with necessary diagrams.

OR

Explain the working of edge-triggered JK flip-flop with necessary diagrams.

Roll No: _____

Sign of Supervisor: _____

Marks: _____



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Date: 23-09-2025 Tuesday

Time: 20 Min.

Marks: 15

Quiz B.Sc. Semester-5 (NEP)

Q.1 Fill in the blanks with correct answer. Each of 1 Mark. (8)

- (i) With increase in frequency, the capacitive reactance..... (decreases / increases)
- (ii) The ratio of output voltage to the input voltage is called as ... (power/gain).
- (iii) The input impedance of ideal op-amp is (zero / infinite).
- (iv) An integrator converts a sin wave into a..... (triangular/ cosine)
- (v) A nibble is a string of bits. (4 / 6)
- (vi) The NAND gate and NOR gate are called..... logic gates. (basic/universal)
- (vii) A Flip-flop can be used to store..... bit. (1 / 2)
- (viii) In a Mod-10 ripple counter..... flip-flops are used. (3 / 4)



Q.2 Answer with True or False. Each of 1 Mark (7)

- (i) In high frequency region, gain decreases due to coupling capacitors. []
- (ii) In class B operation output current flows for full cycle of input. []
- (iii) Op-amp can be used as logarithmic amplifier. []
- (iv) Gain of a summing amplifier is 1. []
- (v) The binary number system uses only two digits, 0 and 1. []
- (vi) XNOR gate is called the universal logic gate. []
- (vii) Race condition is not possible in D flip-flop (latch). []

=====xyz=====