

**SARDAR PATEL UNIVERSITY**

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**B.Sc. (5<sup>th</sup> Sem) Examination - 2013 [CBCS]**12<sup>th</sup> November, 2013

10:30 am - 1:30 pm

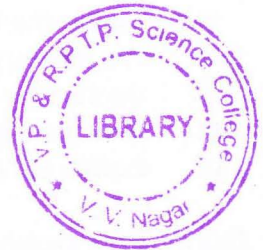
**US05CINS01 (Instrumentation)**

8085 Microprocessor Architecture and Programming - 1

**Maximum Marks: 70**

**Que 1** Each question below gives a multiple choice of answers. Choose the most appropriate [10]  
one.

- 1 Program Counter is \_\_\_\_\_ - bit Register.
  - i. 8
  - ii. 16
  - iii. 32
  - iv. None of the above
- 2 The 74LS245 includes \_\_\_\_\_ Bus Drivers.
  - i. 4
  - ii. 8
  - iii. 16
  - iv. None of the above
- 3 Crystal frequency of 8085 uP is \_\_\_\_\_.
  - i. 3 KHz
  - ii. 6 KHz
  - iii. 3 MHz
  - iv. None of the above
- 4 ADI is \_\_\_\_\_ - byte instruction.
  - i. 1
  - ii. 2
  - iii. 3
  - iv. None of the above
- 5 \_\_\_\_\_ Flag is affected during Data Transfer Operations.
  - i. Carry
  - ii. Zero
  - iii. Sign
  - iv. None of the above
- 6 The Data Bus is a group of \_\_\_\_\_ lines.
  - i. 4
  - ii. 8
  - iii. 16
  - iv. None of the above
- 7 \_\_\_\_\_ Signal is used to delay the uP Read or Write cycles until a slow - responding peripheral is ready to send or accept data.
  - i. HOLD
  - ii. RESET OUT
  - iii. READY
  - iv. None of the above
- 8 NOP is \_\_\_\_\_ byte instruction.
  - i. 1
  - ii. 2
  - iii. 3
  - iv. None of the above
- 9 If zero flag is 1, then \_\_\_\_\_ flag is also 1.
  - i. Carry
  - ii. Zero
  - iii. Sign
  - iv. None of the above
- 10 The Address Bus is a group of \_\_\_\_\_ lines.
  - i. 8
  - ii. 12
  - iii. 14
  - iv. None of the above



P.T.O

**Que 2 Short Questions (Attempt any TEN)**

**[20]**

- 1 What is Compiler?
- 2 Explain Memory - Mapped I/O.
- 3 If 8085 adds  $87_H$  and  $79_H$ , specify the contents of the accumulator and the status of the S, Z, and CY flags.
- 4 What operation can be performed by using the instruction SUB A? Specify the status of Z and CY.
- 5 What is an Interpreter?
- 6 Specify the number of registers and memory cells in a  $128 \times 4$  memory chip.
- 7 If the clock frequency is 5 MHz, how much time is required to execute 18 T - states?
- 8 What operation can be performed by using the instruction XRA A? Specify the status of Z and CY.
- 9 Explain the function of Program Counter and Stack Pointer.
- 10 The memory address of the last location of a 1K byte memory chip is given as  $FBFF_H$ . Specify the starting address.
- 11 Draw schematic to generate Read/Write Control Signals for Memory and I/O.
- 12 Explain SUI Instruction.

**Que 3 [A] Explain 8085 Programming Model. [05]**

**[B] Explain the difference between the Machine Language and the Assembly Language of the 8085 microprocessor. What is an Assembler? What are Low - and High Level Languages? [05]**

**OR**

**[C] Give 8085 Instruction Classification. [05]**

**[D] Write a note on Data Format. [05]**

**Que 4 [A] Discuss Peripheral - Mapped I/O. [05]**

**[B] Give an account of Encoder. [05]**

**OR**

**[C] Explain Octal Bus Transceiver with necessary Logic Diagram and Function Table. [05]**

**[D] Write a note on Microprocessor - Initiated Operations and 8085 Bus Organization. [05]**

**Que 5 [A] Write a detailed note on 8085 Microprocessor. [10]**

**OR**

**[B] Explain the need to Demultiplex the bus  $AD_7 - AD_0$ . [05]**

**[C] With necessary Timing Diagram, explain how byte from memory is transferred to MPU. [05]**

**Que 6 [A] Write a program to perform the following functions: [05]**

Load the number  $FB_H$  in register E. Load the number  $C9_H$  in register B. Increment the contents of register C by one. Add the contents of registers B and E and display the sum at output PORT1.

**[B] Write instructions to load  $65_H$  in register C, and  $92_H$  in A. Display the  $65_H$  at PORT0 and  $92_H$  at PORT1. [05]**

**OR**

**[C] Write a program to do the following: [05]**

Load the number  $40_H$  in register C and  $A9_H$  in register D. Subtract  $A9_H$  from  $40_H$ . Display the answer at PORT1.

**[D] Load the data byte  $A8_H$  in register C, mask the high - order bits ( $D_7 - D_4$ ), and display the low - order bits ( $D_3 - D_0$ ) at an output port. [05]**

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